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(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
1006, Oaza Kadoma
Kadoma-shi, Osaka-fu, 571(JP)

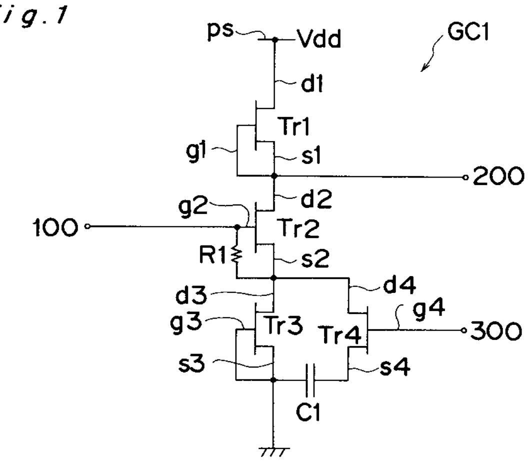
(72) Inventor: **Kunihisa, Taketo**
17-11, Shimizu-cho
Neyagawa-shi, Osaka-fu(JP)
Inventor: **Sakai, Yukio**
70-182, Nojiri-cho
Sakai-shi, Osaka-fu(JP)
Inventor: **Yahata, Kazuhiro**
2-2-30, Ooimazato, Higashinari-ku
Osaka-shi, Osaka-fu(JP)
Inventor: **Nakatsuka, Tadayoshi**
5-30, Ookiri 4-chome, Higashiyodogawa-ku
Osaka-shi, Osaka-fu(JP)
Inventor: **Yagita, Hideki**
13-7, Kitafunabashi-cho
Hirakata-shi, Osaka-fu(JP)

(74) Representative: **Eisenführ, Speiser & Partner**
Martinistrasse 24
W-2800 Bremen 1 (DE)

(54) Gain control circuit and semiconductor device.

(57) A gain control circuit (GC1) includes a first FET (Tr1) for serving as an active load, a second FET (Tr2) serving as an amplifier, and a third FET (Tr3) for serving as a current source. The first, second, and third FETs (Tr1, Tr2, and Tr3) have substantially the same characteristics and are mutually connected in a series. The gain control circuit (GC1) further includes a fourth FET (Tr4) for serving as a variable active load connected in parallel with the third FET (Tr3) and a capacitor (C1) connected between the third and fourth FETs (Tr3 and Tr4). The fourth FET (Tr4) is also connected to a gain control terminal (300). The gain of the second FET (Tr2) is controlled by the voltage applied to the gate (g4) of the fourth FET (Tr4) through said gain control line (300).

Fig. 1



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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a gain control circuit using a metal semiconductor field-effect transistor (MESFET) device of gallium arsenide (GaAs) that bay be used in television tuners. The present invention also relates to a semiconductor device.

2. Description of the Prior Art

Gain control circuits conventionally used in television tuners generally control the gain using a device combining P-I-N diode attenuator and fixed gain amplifier, or by changing the operating point of a dual gate FET device. Cost effective commercial application of P-I-N diodes is impeded, however, by the difficulties of manufacturing a P-I-N structure with stable characteristics from GaAs. When a gain control circuit using dual gate FET devices is used, the drain current (hereinafter referred to as "I_{DS}") varies with the change in the operating point. This necessitates, as described in IEEE Transactions on Consumer Electronics (Vol. 53, No. 3, August 1989), a separate circuit to stabilize the DC bias and to stabilize the variation in current consumption of the overall gain control circuit due to the gain control voltage. IEEE is an abbreviation for Institute of Electrical and Electronics Engineers, Inc.

In a semiconductor device integrating devices such as GaAs MESFET devices with high I_{DS} variation to form a gain control circuit, the DC bias of the drain will fluctuate as the voltage drop changes with the variation in I_{DS} if a resistance load is used between the power supply and drain of the source ground amplifier. Furthermore, while the drain load resistance must be increased to obtain a sufficient gain, this also produces a larger change in the DC bias of the drain. As a result, a drain-source voltage (hereinafter referred to as "V_{DS}") sufficient to assure operation of the FET in the saturation range is set in the conventional semiconductor device when the power supply voltage is low, and it is difficult to simultaneously obtain sufficient gain and a stable DC bias.

In addition, a gain control circuit with a circuit construction which does not require a special power supply to set the gain control voltage and does not require a power supply providing a negative voltage is desirable for general purpose applicability. This type of circuit construction requires that the voltage range needed to obtain both the maximum and minimum gain levels be within the power supply voltage to ground voltage range of the gain control circuit, a requirement which cannot be met with the conventional gain control circuit construction.

SUMMARY OF THE INVENTION

The object of the present invention is therefore to provide a gain control circuit which solves these problems.

The present invention has been developed with a view to substantially solving the above described disadvantages and has for its essential object to provide an improved gain control circuit.

In order to achieve the aforementioned objective, a gain control circuit comprises a first FET for serving as an active load connected to a power supply line; a second FET, connected to a gain control line, for serving as an amplifier arranged in a series connection with the first FET; a third FET for serving as a current source arranged in a series connection with said second FET; a fourth FET for serving as a variable active load arranged in a parallel connection with the third FET and in connection with a gain control line; and a capacitor connected between the third and fourth FETs, whereby the gain of the second FET is controlled by the voltage applied to the gate of the fourth gate through the gain control line.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings throughout which like parts are designated by like reference numerals, and in which:

Fig. 1 is a circuit diagram of a gain control circuit according to a first embodiment of the invention;

Fig. 2 is a circuit diagram of a gain control circuit according to a second embodiment of the invention;

Fig. 3 is a circuit diagram of a gain control circuit according to a third embodiment of the invention;

Fig. 4 is a circuit diagram of a first semiconductor device according to the first embodiment of the present invention;

Fig. 5 is a circuit diagram of a second semiconductor device according to the second embodiment of the present invention;

Fig. 6 is a circuit diagram of a third semiconductor device according to the third embodiment of the present invention,

Fig. 7 is a graph of the maximum saturation drain current dependency of the output terminal bias in the gain control circuit shown in Fig. 1;

Fig. 8 is a graph of the gain control voltage dependency of the gain in the gain control circuit shown in Fig. 1;

Fig. 9 is a graph of the maximum saturation drain current dependency of the output terminal bias in the gain control circuit shown in Fig. 2;

Fig. 10 is a graph of the gain control voltage dependency of the gain in the gain control circuit shown in Fig. 2;

Fig. 11 is a graph of the maximum saturation drain current dependency of the output terminal bias in the gain control circuit shown in Fig. 3;

Fig. 12 is a graph of the gain control voltage dependency of the gain in the gain control circuit shown in Fig. 3;

Fig. 13 is a graph of the gain control voltage dependency of the gain in the first semiconductor device shown in Fig. 4;

Fig. 14 is a graph of the gain compression dependency of the third order intermodulation distortion suppression ratio in the first semiconductor device shown in Fig. 4;

Fig. 15 is a graph of the gain control voltage dependency of the gain in the second semiconductor device shown in Fig. 5;

Fig. 16 is a graph of the gain compression dependency of the third order intermodulation distortion suppression ratio in the second semiconductor device shown in Fig. 5;

Fig. 17 is a graph of the gain control voltage dependency of the gain in the third semiconductor device shown in Fig. 6;

Fig. 18 is a graph of the gain compression dependency of the third order intermodulation distortion suppression ratio in the third semiconductor device shown in Fig. 6;

Fig. 19 is an equivalent circuit diagram of the gain control circuit shown in Fig. 1;

Fig. 20 is an equivalent circuit diagram of the gain control circuit shown in Fig. 2;

Fig. 21 is an equivalent circuit diagram of the gain control circuit shown in Fig. 3;

Fig. 22 is an equivalent circuit diagram Of the semiconductor device shown in Fig. 4;

Fig. 23 is an equivalent circuit diagram of the semiconductor device shown in Fig. 5; and

Fig. 24 is an equivalent circuit diagram of the semiconductor device shown in Fig. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1, a gain control circuit according to a first embodiment of the present invention is shown. The gain control circuit GC1 comprises four field effect transistors (hereinafter referred to as "FET"). The first FET Tr1 is used as an active load, the second FET Tr2 is used as an amplifier, the third FET Tr3 as a rated current source, and the fourth FET Tr4 as a variable active load. It is important to note that the first, second, and third FETs, Tr1, Tr2, and Tr3 have substantially the same characteristics.

The gain control circuit GC1 further comprises a bias-setting damping resistor R1, a high frequency ground capacitor C1, an input terminal 100, an output terminal 200, a gain control terminal 300, and a power supply line ps.

In the gain control circuit GC1, the first FET Tr1 has a drain line d1 connected to the power source line ps and source and gate lines s1 and g1 connected to a drain line d2 of the second FET Tr1. The bias-setting damping resistor R1 is connected between gate and source lines s2 and g2 of the second FET Tr2. The source line s2 of the second FET Tr2 is connected to the drain lines d3 and d4 of the third FET Tr3 and fourth FET Tr4. A gate line g3 and source lines s3 of the third FET Tr3 are grounded. The high frequency ground capacitor C1 is connected between a source line s4 of the fourth FET Tr4 and the ground.

The gate and drain lines g2 and d2 of the second FET Tr2 are connected to the input and output lines 100 and 200, respectively, and the gate line g4 of the fourth FET Tr4 is connected to the gain control terminal 300. The gain of the second FET Tr2, which serves as an amplifier, is changed by varying the voltage impressed to the gain control terminal 300.

The operation of the gain control circuit GC1 differs between the DC bias component and the RF component.

First, the operation of the circuit GC1 with respect to the DC bias is described. The resistance of the bias-setting damping resistor R1 is set within the range of some hundreds ohms to some kilo ohms go that the voltage drop of the bias-setting damping resistor R1 caused by the gate leakage current of the second FET Tr2 is sufficiently low. The maximum saturation drain current (hereinafter referred to as "I_{DSS}") of the third FET Tr3 through line d3 is set to approximately one hundred times the current flowing through line d4. As a result, the circuit is self-biased such that the same I_{DSS} of the third FET Tr3 flows to the first and second FETs Tr1 and Tr2. Also, the drain-source voltage (hereinafter referred to as "V_{DS}") is equal in these three FETs Tr1, Tr2, and Tr3, and the gate-source voltage (hereinafter referred to as "V_{GS}") is also equal in these three FETs Tr1, Tr2, and Tr3. As a result, the voltage of the output terminal 200 is two-thirds (2/3) of the power supply voltage V_{dd} - (hereinafter referred as "V_{dd}"), and the source voltage of the second FET Tr2 is one-third (1/3) of the V_{dd} regardless of the value of I_{DES}.

Next, the operation of the gain control circuit GC1 with respect to the high frequency (RF) characteristics is described. The total impedance Zt between the ground and the source line s2 of the second FET Tr2, which is a source commoned amplifier, is determined by the drain input impedance Z3 of the third FET Tr3, the drain input impedance Z4 of the fourth FET Tr4 drain input impedance, and the impedance Zc of the capacitor C1, and is obtained as follows:

$$Zt = Z3 \times (Z4 + Zc) /(Z3 + Z4 + Zc).$$

If, for example, the gate length ℓg = 1 μm, gate width wg = 250 μm, and the threshold voltage Vth = 0.4 V, the third FET Tr3 drain input impedance will he high, approximately 700 Ω. Relative to this, the high frequency ground capacitor C1 has a low impedance, e.g., 1 Ω for a 100 pF with respect to a 1 GHz signal. As a result, the total impedance Zt is mostly controlled by the drain input impedance Z4 of the fourth FET Tr4.

The fourth FET Tr4 drain input impedance is obtained when V_{DS} = 0 V, but is varied by the gate-drain voltage (hereinafter referred to as "V_{GD}") thereof. For example, if the gate length ℓg = 1 μm, gate width wg = 400 μm, and the threshold voltage Vth = 0.4 V, the fourth FET Tr4 drain input impedance may vary between 250 Ω to 20 Ω with respect to the V_{GD} range -0.4 V to 0 V. As a result, the impedance of the third FET Tr3, serving as a bypass, can be changed by controlling the fourth FET Tr4 gate voltage, and thus, the gain of FET Tr2 serving as amplifier can be controlled.

The impedance of the first FET Tr1, which serves an active load, is high (approximately 700 Ω) because the same signal is input to both the source and gate lines s1 and g1. In other words, the load connected to the drain of the second FET Tr2, i.e., the amplifier, is high, and sufficient gain can therefore be obtained. When this load is substituted by a resistance load, a voltage drop of 7 V occurs when I_{DSS} is 10 mA, but by using the first FET Tr1 as an active load, the potential difference can be limited to approximately 1.6 v. Variations in the DC bias can thus be prevented.

Referring to Fig. 19, an equivalent circuit of the gain control circuit GC1 with respect to AC signal is shown. It is to be noted that the bias-setting damping resistor R1 can be substituted by an inductor L1 which can cut the high frequency component.

Referring to Figs. 7 and 8, the maximum saturation drain current dependency of the output terminal bias and the gain control voltage dependency of the gain in the gain control circuit GC1 are described below. The characteristics represented in these figures are obtained from the experiments. The experiments are executed under the conditions that the V_{dd} is 5 V, the voltage applied to the gain control terminal 300, i.e., the gain control voltage, is from 1.0 - 1.6 V, the gate width wg of each of the first, second, and third FETs Tr1, Tr2, and Tr3 is 250 μm, the gate width wg of the fourth FET Tr4 is 400 μm, the bias-setting damping resistance R1 is 1 kΩ, the high frequency ground capacitance C1 is 1000 pF, and the used frequency is 100 MHz.

As shown in Fig. 7, a stable bias level is observed at 3.3 V throughout the maximum saturation drain current I_{DSS} from 4.9 to 12.5,mA, provided that the gain control voltage is 1.5 V.

As shown in Fig. 8, with the circuit GC1 of Fig. 1 it is possible to control the gain from +34 dB to +5 dB with respect to the gain control voltage from 1.0 V to 1.6 V. In other words, the variation from the voltage for obtaining the maximum gain to the voltage for obtaining the minimum gain is between the power supply voltage and the ground voltage of the gain control circuit. Thus, it is not necessary to provide a separate power supply for controlling the gain. It is to be noted that the maximum saturation drain current I_{DSS} obtained in the above case is 8.3 mA.

Referring to Fig. 2, a gain control circuit according to a second embodiment of the present invention is described. The gain control circuit GC2 comprises a first FET Tr11 serving as an active load, a second FET Tr12 serving as an amplifier, and a third FET Tr13 serving as a variable active load. The first and second FETs, Tr11 and Tr12 have substantially the same characteristics. The gain control circuit GC2 further comprises a bias-setting damping resistor R11, a choke coil L11, a high frequency ground capacitor C11, an input terminal 100, an output terminal 200, a gain control terminal 300, and a power supply line ps.

In the gain control circuit GG2, a drain line d11 of the first FET Tr11 is connected to the power supply line ps, and Source and gate lines s11 and g11 are connected each other. The capacitor C11 is connected between the power supply line ps and the source line s11 of the first FET Tr11. a source line s13 of the third FET Tr13 is connected to a drain line d12 of the second FET Tr12. The choke coil L11 is connected between the drain and Source lines d13 and s13 of the third FET Tr13.

The bias-setting damping resistor R11 is connected between a gate line g12 of the second FET Tr12 and the ground, and a source line s12 of the second FET Tr12 is grounded.

The gate line g12 and drain line d12 of the second FET Tr12 are connected to the input terminal 100 and output 200 terminal, respectively, and the gate line g13 of the third FET Tr13 is connected to the gain control terminal 300. The gain of

the second FET Tr12, which serves as an amplifier, is changed by varying the voltage applied to the gain control terminal 300.

First, the operation of the circuit GC2 with respect to the DC bias is described below. The resistance of the bias-setting damping resistor R11 is set within the range of some hundreds ohms to some Kilo ohms so that the voltage drop caused by the gate leakage current of the second FET Tr12 at the bias-setting damping resistor R11 is sufficiently low. The I_{DSS} of the second FET Tr12 through line d12 is set to approximately one hundred times the current flowing through the line g13. As a result, the circuit GC2 is self-biased such that the I_{DRS} of the second FET Tr12 flows to the first FET Tr11, the V_{DS} is equal in the first and second FETs Tr11 and Tr12, and the V_{GS} is also equal in these two FETs Tr11 and Tr12. Thus, the voltage of the output terminal 200 is one-half (1/2) of the V_{dd}regardless of the value of I_{DSS}.

Next, the operation of the gain control circuit GC2 with respect to the RF characteristics is described below. The total impedance Zt between the power supply line ps and the drain line d12 is determined by the source input impedance Z13, and the impedance $Z\ell$ of the choke coil L11, the source input impedance Z11 of the first FET Tr11, and the impedance Zc of the capacitor C11, and is obtained as follows:

$$Zt = Z11 \times Zc / (Z11 + Zc) + Z13 X Z\ell / Z13 + Z\ell.$$

It is noted that the second FET Tr12 and the power supply ps serve as a source-grounded amplifier and a high frequency ground, respectively. The source input impedance of the first FET Tr11 is high because the same signal is input to the source and gate lines s11 and g11 of the first FET Tr11.

If, for example, the gate length $\ell g = 1\ \mu m$, gate width $wg = 250\ \mu m$, and the threshold voltage $Vth = 0.4$ V, the source input impedence of the first FET Tr11 will be approximately 700 Ω. In addition, if the capacitance of the high frequency ground capacitor C11 with respect to a 1 GHz signal is 100 pF, the impedance will be a low 10 Ω. As a result, the total impedance Zt will be less than 10 Ω. If the inductance of the choke coil L11 with respect to a 1 GHz signal is 1 μH, the total impedance Zt will be 1 kΩ. As a result, the total impedance Zt is mostly controlled by the source input impedance Z13 of the third FET Tr13.

The third FET Tr13 source input impedance is obtained when V_{DS} is 0 V, but varies with respect to the value of the V_{GS} thereof. For example, if the gate length $\ell g = 1\ \mu m$, gate width $wg = 400\ \mu m$, and the threshold voltage $Vth = 0.4$ V, the impedance may vary between 250 Ω to 20 Ω with respect to the V_{GS} range -0.4 V to 0 V. As a result, the impedance of the second FET Tr12, serving as a drain load, can be changed by controlling the voltage applied to the gate line g13 of third FET Tr13, and thus, the gain of the FET Tr12 serving as an amplifier can be controlled.

As described above, the impedance of the first FET Tr11, which serves an active load, is high, approximately 700 Ω. In other words, the load connected to the drain of the second FET Tr12, i.e., the amplifier, is high, and sufficient gain can therefore be obtained. When this load is substituted by a resistance load, a voltage drop of 7 V occurs when I_{DSS} is 10 mA, but by using the first FET Tr11 as an active load, the potential difference can be limited to approximately 2.5 V. Variations in the DC bias can thus be prevented. In Fig. 20, an equivalent circuit of the gain control circuit GC2 with respect to AC signal is shown.

Referring to Figs. 9 and 10, the maximum saturation drain current dependency of the output terminal bias and the gain control voltage dependency of the gain in the gain control circuit GC2 are described below. The characteristics represented in these figures are obtained from the experiments. The experiments are executed under the conditions that the V_{dd} is 5 V, the voltage applied to the gain control terminal 300, i.e., the gain control voltage, ranges from 2.0 - 2.5 V, the gate width wg of each of the first, second, and third FETs Tr11, Tr12, and Tr13 is 250 μm, the bias-setting damping resistance R11 is 1 kΩ, the high frequency ground capacitor C11 is 1000 Pf, the choke coil L11 inductance is 1 μH, and the used frequency is 100 MHz.

As shown in Fig. 9, a stable bias level is at 2.5 V throughout the maximum saturation drain current I_{DSS} from 5.1 to 13.0 mA, provided that the gain control voltage is 2.5 V.

As shown in Fig. 10 with the circuit GC2 of Fig. 2, it is possible to control the gain from +35 dB to +8 dB with respect to the gain control voltage from 2.0 V to 2.5 V. In other words, the variation form the voltage range for obtaining the maximum gain to the voltage for obtaining the minimum gain is between the power supply voltage and the ground voltage of the gain control circuit. Thus it is not necessary to provide a separate power supply for controlling the gain. It is to be noted that the maximum saturation drain current I_{DSS} obtained in the above case is 8.7 mA.

It is to be noted that the high frequency ground capacitor C11 is connected between the power supply and the source line of the first FET Tr11 in the second embodiment described above, but the same effect can be obtained by connecting it between the ground and the source line of the first

FET Tr11.

Referring to Fig. 3, a gain control circuit according to a third embodiment of the present invention is described. The gain control circuit GC3 comprises three FETs. The first FET Tr21 is used as an active load, the second FET Tr22 is used as an amplifier, and the third FET Tr23 as a variable active load. The first and second FETs, Tr21 and Tr22 have substantially the same characteristics.

The gain control circuit further comprises a bias-setting damping resistor R21, a coupling capacitor C21, an input terminal 100, an output terminal 200, a gain control terminal 300, and a power supply line ps. A drain line d21 of the first FET Tr21 is connected to the power supply line ps, and a source line s21 and a gate line g21 are connected to a drain line d22 of the second FET Tr22. The bias-setting damping resistor R21 is connected between a gate line g22 of the second FET Tr22 and the ground, and a source line s22 of the second FET Tr22 is grounded. A drain line d23 of the third FET Tr23 is connected to the drain line d22 of the second FET Tr22. The coupling capacitor C21 is connected to a source line s23 of the third FET Tr23 and the gate line g22 of the second FET Tr22.

The gate line g22 and drain lines d22 of the second FET Tr22 are connected to the input terminal 100 and output terminal 200, respectively, and a gate line g23 of the third FET Tr23 is connected to the gain control terminal 300. The gain of the second FET Tr22, which serves an amplifier, is changed by varying the voltage applied to the gain control terminal 300.

First, the operation of the gain control circuit GC3 with respect to the DC bias is described below. The resistance of the bias-setting damping resistor R21 is set so that the voltage drop caused by the gate leakage current of the second FET Tr22 at the bias-setting damping resistor R21 is sufficiently low. The I_{DSS} of the second FET Tr22 through the line d22 is set to approximately one hundred times the current flowing through the line g23. As a result, the circuit is self-biased such that the same I_{DSS} of the second FET Tr22 flows to the first FETs Tr21. Also, the drain-source voltage V_{DS} is equal in the first and second FETs Tr21 and Tr22, and the gate-source voltage V_{GS} is also equal in these two FETs. As a result, the voltage of the output terminal 200 is one-half (1/2) of the V_{dd} regardless of the value of I_{DSS}.

Next, the operation of the gain control circuit GC3 with respect to the RF characteristics is described below. The total feedback impedance Zt between the drain line d22 and gate lines g22 of the second FET Tr22, which serves as a source-grounded amplifier, is determined by the impedance Z23 between the drain line d23 and source line s23 of the third FET Tr23 and the impedance Zc of the coupling capacitor C21, and is obtained as follows:

$$Zt = Z23 + Zc.$$

Zt is mostly controlled by the impedance Z23, because the impedance Zc is low, e.g., 10 Ω when the capacitance to a 1 Ghz signal is 100 Pf.

The third FET Tr23 source input impedance is the impedance when V_{DS} is 0 V, but varies with the value of the gate-source voltage V_{GS}. For example, if the gate length ℓg = 1 μm, gate width wg = 400 μm, and the threshold voltage Vth = 0.4 V, the impedance will vary between 250 Ω to 20 Ω through the V_{GS} range -0.4 V to 0 V. As a result, the feedback from the drain line d22 to the gate line g22 of the second PET Tr22 can be changed and the gain can be controlled by controlling the third FET Tr23 gate voltage.

The impedance of the first PET Tr21, which serves an active load, is high (approximately 700 Ω) because the same signal is input to both the source and gate lines s21 and g21. In other words, the load connected to the drain of the second FET Tr22, i.e., the amplifier, is high, and sufficient gain can therefore be obtained. When this load is substituted by a resistance load, a voltage drop of 7 V occurs when I_{DSS} is 10 mA, but by using the first PET Tr21 as an active load, the potential difference can be limited to approximately 2.5 V. Variations in the DC bias can thus be prevented. In Fig. 21, an equivalent circuit of the gain control circuit Gc3 with respect to AC signal is shown.

Referring to Figs. 11 and 12, the maximum saturation drain current dependency of the output terminal bias and the gain control voltage dependency of the gain in the gain control circuit GC3 are described below. The characteristics represented in these figures are obtained from the experiments. The experiments are executed under the conditions that the V_{dd} is 5 V, the voltage applied to the gain control terminal 300, i.e., the gain control voltage, is from 2.0 - 2.5 V, the gate width wg of each of the first, second, and third FETs Tr21, Tr22, and Tr23 is 250 μm, the bias-setting damping resistance R21 is 1 kΩ, the coupling capacitor C21 is 1000 Pf, and the used frequency is 100 MHz.

As shown in Fig. 11, a stable bias level at 2.5 V throughout the I_{DSS} from 5.1 to 13.0 mA, provided that the gain control voltage is 2.5 V.

As shown in Fig. 12, with the circuit GC3 of Fig. 3, it is possible to control the gain from +37 dB to -15 dB with respect to the gain control voltage from 2.0 V to 2.5 V. In other words, the variation from the voltage for obtaining the maximum gain to the voltage for obtaining the minimum

gain is between the power supply voltage and the ground voltage of the gain control circuit GC3. Thus, it is not necessary to provide a separate power supply for controlling the gain. It is to be noted that the I_{DSS} obtained in the above case is 8.7 mA.

Referring to Fig. 4, a circuit diagram of a semiconductor device based on the gain control circuit GC1 according to the first embodiment shown in Fig. 1 is shown. The semiconductor device SGC1 is an integrated circuit device in which the major part of the gain control circuit GC1 of the present invention is assembled. In addition to the circuit shown in Fig. 1, the semiconductor device SGC1 shown in Fig. 4 has a fifth FET Tr5 as a source follower, a sixth FET Tr6 as a rated current source, a gain clamp resistor R2, and a current clamp resistor R3. The power supply line ps and the ground terminal are substituted by a power supply terminal 600 and a ground terminal 500, respectively. It is to be noted that the high frequency ground capacitor C1 is externally provided between a high frequency ground terminal 400 and any one of the ground terminal 500, the power supply terminal 600, or other high frequency ground point.

The fifth FET Tr5 has a drain line d5 connected to the drain line d1 of the first FET Tr1, a gate line g5 connected to the gate line g1 and the source line s1 of the first FET Tr1, and a source line s5 connected to the output terminal 200, as shown. The sixth FET Tr6 has a drain line d6 connected to the output terminal 200, and has a gate line g6 and a source line s6 which are connected to the ground terminal 500. Thus, the fifth FET Tr5 and sixth FET Tr6 function as a source follower and a rated current source, respectively.

The gain clamp resistor R2 is connected between the drain line d4 and the source line s4 of the fourth FET Tr4. The current clamp resistor R3 is connected between the gate line g4 of the fourth FET Tr4 and the gain control terminal 300.

The semiconductor device SGC1, when compared with the gain control circuit GC1 described with respect to Fig. 1, has the high capacitance capacitor C1 externally connected because it is difficult to assemble the capacitor in the integrated circuit. Also, the source follower FET Tr5 is added as an output buffer, and both gain clamp resistor R2 and current clamp resistor R3 are added. Therefore, as with the gain control circuit GC1, the first, second, and third FETs Tr1, Tr2, and Tr3 are self-biased to the same characteristics as described above. The voltage of the output terminal 200 is therefore fixed to two-thirds (2/3) of the V_{dd} regardless of the I_{DSS}, and the source voltage of the second FET Tr2 is fixed at one-third (1/3) of the V_{dd}. The impedance of the third FET Tr3 bypass can be changed. Thus, the gain can be controlled by controlling the gate voltage of the fourth FET Tr4.

The change in the bias level of the output terminal 200 is described. The gate-source voltage V_{GS} results from the maximum saturation drain current I_{DSS} because the fifth FET Tr5 is driven by the I_{DSS} of the sixth FET Tr6. The value of this voltage depends upon the change in the sixth FET Tr6 I_{DSS},but the change in I_{DS} to the variation in the V_{GS} is small. For example, if the gate length ℓg = 1 μm, gate width wg = 500 μm, the threshold voltage Vth = 0.4 V, and the conductance gm is 100 mS, the V_{GS} will change only 0.1 V even if there is a 10 mA change in the sixth FET Tr6 I_{DSS}. This is an extremely stable bias level considering the operation of the fifth and sixth FETs Tr5, Tr6 at the saturation range, and is possible because the fifth FET Tr5 gate voltage is fixed at two-thirds of the V_{dd}.

In addition, the gain clamp resistor R2 is used to prevent deterioration of the third order intermodulation distortion characteristics caused by the bypass impedance being too high. The current clamp resistor R3 provides both a direct current control function and a high frequency characteristic control function. With respect to direct current, when the voltage difference between the gain control terminal 300 and the source line s2 of the second FET Tr2 becomes greater than the Schottky barrier, there is a large current flow from the fourth FET Tr4 gate to the third FET Tr3. To prevent this, the current clamp resistor R3 drops the voltage and lowers the gate potential of the fourth FET Tr4. With respect to high frequency characteristics, the current clamp resistor R3 inhibits signal leaking through the drain-gate capacity of the fourth FET Tr4 to the gain control terminal 300. As a result, by inserting the current clamp resistor R3 between the fourth FET Tr4 gate line and the gain control terminal 300, fluctuations in the DC bias can be easily prevented, gate damage caused by forward current can be avoided, and the high frequency characteristics can be improved. In addition, a stable power supply to the load can be maintained because the fifth FET Tr5 is a source follower that reduces the output impedance across a wide band width. In Fig. 22, an equivalent circuit of the semiconductor device SGC1 is shown. It is to be noted that the fifth and sixth FETS Tr5 and Tr6 are functioning as an impedance matching.

Referring to Figs. 13 and 14, the gain control voltage dependency of the gain and the gain compression dependency of the third order intermodulation distortion product suppression ratio (herein after referred to as "IMD3") in the semiconductor device SGC1 are described. It is to be noted that the third order intermodulation distortion

product is a byproduct signal when the two different signals are input to the circuit. IMD3 represents how this byproduct signal is suppressed. The characteristics represented in these figures are obtained from the experiments executed under the conditions that the power supply voltage is 5 V, the gain control voltage applied to the gain control terminal 300 is varied from 1.2 to 2.0 V, the gate width wg of each of the first, second, third, and fifth FETs Tr1, Tr2, Tr3, Tr5 is 250 μm, the gate width wg of the fourth FET Tr4 is 400 μm, the gate width wg of the sixth FET Tr6 is 500 μm, the bias setting damping resistor R1 is 1 kΩ, the gain clamp resistor R2 is 1 kΩ, the current clamp resistance R3 is 10 kΩ, and the 1000 pF high frequency ground capacitor is connected between the high frequency ground terminal 400 and the ground terminal 500.

As shown in Fig. 13, with the semiconductor device SGC1 of Fig. 4, it is possible to control the gain from +24 dB to +4 dB with respect to the gain control voltage from 1.0 V to 1.6 V. In other words, the variation from the voltage for obtaining the maximum gain to the voltage for obtaining the minimum gain is between the power supply voltage and the ground Voltage of the semiconductor device SGC1. Thus, it is not necessary to provide a separate power supply for controlling the gain. It is to be noted that the measured frequency is 400 MHz, and the maximum saturation drain current I_{DSS} obtained in the above case is 8.3 mA.

The gain compression dependency of the IMD3 is shown in Fig. 14, in which the third order intermodulation distortion product of 350 MHz when two signals (400 MHz and 450 MHz) are input at a -30 dBm input level is employed. The output component when a 400 MHz signal is input at a -30 dBm input level is employed as a signal component. As shown in Fig. 14, third order intermodulation distortion product performance of greater than 60 dBc is obtained within a range from zero to 15 dB of gain compression.

Referring to Fig. 5, a circuit diagram of semiconductor device based on the gain control circuit GC2 according to the second embodiment shown in Fig. 2 is shown. The semiconductor device SGC2 is an integrated circuit device in which the major part of the gain control circuit CG2 of the present invention is assembled. In addition to the circuit shown in Fig. 2, the semiconductor device SGC2 shown in Fig. 5 has a fourth FET Tr14 as a source follower, a fifth FET Tr6 as a rated current source, and a current clamp resistance R12. The power supply line ps and the ground terminal are substituted by a power supply terminal 600 and a ground terminal 500, respectively. It is to be noted that the choke coil L11 and high capacity high frequency ground capacitor C11 is externally provided between a high frequency ground terminal 400 and any one of the ground terminal 500, the power supply terminal 600, or other high frequency ground point. A choke coil (not shown) is also connected externally to the high frequency ground terminal 400 and a choke coil terminal 700.

The fourth FET Tr14 has a drain line d14 connected to the drain line d11 of the first FET Tr11, a gate line g14 connected to the source line s13 of the third FET Tr13, and a source line s14 connected to the output terminal 200, as shown. The fifth FET Tr5 has a drain line d15 connected to the source line s14 of the fourth FET Tr14, and has a gate line g15 and a source line s15 which are connected to the ground terminal 500. Thus, the fourth FET Tr14 and the fifth FET Tr15 function as a source follower and a rated current source, respectively.

The current clamp resistance R12 is connected between the gate line g13 of the third FET Tr13 and the gain control terminal 300.

The semiconductor device SGC2, when compared with the gain control circuit GC2 described with respect to Fig. 2, has the choke coil L11 and high capacity high frequency ground capacitor C11, because it is difficult to assemble the coil and capacitor in the integrated circuit. Also, the source follower FET Tr14 is added as an output buffer, and a current clamp resistance R12 are added. Therefore, as with the gain control circuit according to the second embodiment of the invention, the first and second FETs Tr11, Tr12 are self-biased to the same characteristics as described above. The voltage of the output terminal 200 is therefore fixed to one-half (1/2) of the V_{dd} regardless of the I_{DSS}. The load impedance of the second FET Tr12 can therefore be changed. Thus, the gain can be controlled by controlling the gate voltage of the third FET Tr13.

The change in the bias level of the output terminal 200 is described next. The gate-source voltage v_{DS} results from the maximum saturation drain current I_{DSS} because the fourth FET Tr14 is driven by the I_{DSS} of the fifth FET Tr15. The value of this voltage depends upon the change in the fifth FET Tr15 I_{DRS}, but the change in I_{DS} to the variation in the V_{GS} is small. For example, if the gate length ℓg = 1 μm, gate width wg = 500 μm, the threshold voltage Vth = 0.4 V, and the conductance gm is 100 mS, the V_{OS} will change only 0.1 V even if there is a 10 mA change in the fifth FET Tr15 I_{DSS}. This is an extremely stable bias level considering the operation of the fourth and fifth FETs Tr14, Tr15 at the saturation range, and is possible because the fourth FET Tr14 gate voltage is fixed at one-half of the V_{dd}.

The current clamp resistance R12 provides both a direct current control function and a high frequency characteristic control function. With re-

spect to direct current, when the voltage difference between the gain control terminal 300 and the source line of the first FET Tr11 becomes greater than the Schottky barrier, there is a large current flow from the third FET Tr13 gate to the second FET Tr12. To prevent this, the current clamp resistance R12 drops the voltage and lowers the gate potential of the third FET Tr13. With respect to high frequency characteristics, the current clamp resistance R12 inhibits signal leaking through the source-gate capacity of the third FET Tr13 to the gain control terminal 300. As a result, by inserting the current clamp resistance R12 between the third FET Tr13 gate line and the gain control terminal 300, fluctuations in the DC bias can be easily prevented, gate damage caused by forward current can be avoided, and the high frequency characteristics can be improved. In addition, a stable power supply to the load can be maintained because the fourth FET Tr14 is a source follower that reduces the output impedance across a wide band width.

A gain clamp resistance (not shown in the figures) can also be inserted parallel to the choke coil between the high frequency ground terminal 400 and the choke coil terminal 700 to prevent deterioration of the third order intermodulation distortion characteristics caused by the load impedance becoming too high. In Fig. 23, an equivalent circuit of the semiconductor device SGC2 is described. The fourth and fifth FETS Tr4 and Tr5 are functioning as an impedance matching.

Referring to Figs. 15 and 16, the gain control voltage dependency of the gain and the gain compression dependency of the IMD3 in the semiconductor device SGC2 according are described below. The characteristics represented in these figures are obtained from the experiments executed under the conditions that the power supply voltage is 5 V, the voltage applied to the gain control terminal 300, i.e., the gain control voltage, ranges from 2.0 to 2.5 V, the gate width wg of each of the first, second, and third FETs Tr11, Tr12, Tr13 is 250 μm, the gate width wg of the fourth and fifth FETs Tr14, Tr15 is 500 μm, the bias setting damping resistance R11 is 10 kΩ, the external high frequency ground capacitor is 1000 Pf, and the 1 μH inductance choke coil is connected between the high frequency ground terminal 400 and the choke coil terminal 700. A 1 kΩ gain clamp resistance (not shown) is also connected between the high frequency ground terminal 400 and the choke coil terminal 700.

As shown in Fig. 15, with the semiconductor device SGC2 of Fig. 5, it is possible to control the gain from +22 dB to +3 dB with respect to the gain control voltage from 2.0 V to 3.0 V. In other words, the variation from the voltage for obtaining the maximum gain to the voltage for obtaining the minimum gain is between the power supply voltage and the ground voltage of the gain control circuit. Thus, it is not necessary to provide a separate power supply for controlling the gain. It is to be noted that the measured frequency is 400 MHz, and the maximum saturation drain current I_{DSS} obtained in the above case is 8.9 mA.

The gain compression dependency of the IMD3 is shown in Fig. 16. The third order intermodulation distortion product of the 350 MHz produced when two signals (400 MHz and 450 MHz) are input at a -30 dBm input level is employed. The output component when a 400 MHz signal is input at a -30 dBm input level is employed as the signal component. As will be known from Fig. 16, third order intermodulation distortion product performance of greater than 60 dBc is obtained with respect to a gain compression from zero to 10 dB.

Referring to Fig. 6, a circuit diagram of semiconductor device based on the gain control circuit GC3 according to the third embodiment shown in Fig. 3 is shown. The semiconductor device SGC3 is an integrated circuit device in which the major part of the gain control circuit GC3 is assembled. In addition to the circuit GC3 shown in Fig. 3, the semiconductor device SGC3 shown in Fig. 6 has a fourth FET Tr24 as a source follower, a fifth FET Tr25 as a rated current source, a gain clamp resistance R22, and a current clamp resistance R23. The power supply line ps and the ground line are substituted by a power supply terminal 600 and a ground terminal 500, respectively. It is to be noted that the coupling capacitor C21 is externally provided between a coupling capacitor terminal 800 and the input terminal 100.

The fourth FET Tr24 has a drain line d24 connected to the power supply terminal 600, a gate line g24 connected to the drain line d22 of the second FET Tr22, and a source line s24 connected to the drain line d25 of the fifth FET Tr25. The fifth FET Tr25 has a drain line d25 connected to the source line s24 of the fourth FET Tr24, and a gate line g25 and a source line s25 which are connected to the ground terminal 500, as shown.

The semiconductor device SGC3, when compared with the gain control circuit GC3 described with respect to Fig. 3, has the coupling capacitor externally connected because it is difficult to assemble the capacitor in the integrated circuit. Also, the source follower FET Tr24 is added as an output buffer, and a gain clamp resistance R22 and current clamp resistor R23 are added. Therefore, as with the gain control circuit according to the third embodiment of the invention, the first and second FETs Tr21, Tr22 are self-biased as described above so that the V_{DS} is equal in both. The voltage of the output terminal 200 is therefore fixed to one-half (1/2) of the V_{dd} regardless of the I_{DSS}. The

feedback from the drain line to the gate line of the second FET Tr22 can therefore be changed. Thus, the gain can be controlled by controlling the gate voltage of the third FET Tr23.

The change in the bias level of the output terminal 200 is described. The V_{OS} results from the I_{DSS} because the fourth FET Tr24 is driven by the I_{DSS} of the fifth FET Tr25. The value of this voltage depends upon the change in the fifth FET Tr25 I_{DSS}, but the change In I_{DS} to the variation in the V_{OS} is small. For example, if the gate length ℓg = 1 μm, gate width wg = 500 μm, the threshold voltage Vth = 0.4 V, and the conductance gm is 100 ms, the V_{GS} will change only 0.1 V even if there is a 10 mA change in the fifth FET Tr25 I_{DSS}. This is an extremely stable bias level considering the operation of the fourth and fifth FETs Tr24, Tr25 at the saturation range, and is possible because the fourth FET Tr24 gate voltage is fixed at one-half (1/2) of the V_{dd}.

The gain clamp resistor R22 is used to prevent deterioration of the third order intermodulation distortion characteristics resulting from the feedback from the drain to the gate line of the second FET Tr22 being too low.

The current clamp resistor R23 provides both a direct current control function and a high frequency characteristic control function. With respect to direct current, when the voltage difference between the gain control terminal 300 and the drain line of the third FET Tr23 becomes greater than the Schottky barrier, there is a large current flow from the third FET Tr23 gate to the second FET Tr22. To prevent this, the current clamp resistor R23 drops the voltage and lowers the gate potential of the third FET Tr23. With respect to high frequency characteristics, the current clamp resistor R23 inhibits signal leaking through the drain-gate and the drain-source capacity of the third FET Tr23 to the gain control terminal 300. As a result, by inserting the current clamp resistor R23 between the third FET Tr23 gate line and the gain control terminal 300, fluctuations in the DC bias can be easily prevented, gate damage caused by forward current can be avoided, and the frequency characteristics can be improved. In addition, a stable power supply to the load can be maintained because the fourth FET Tr24 is a source follower that reduces the output impedance across a wide band width. In Fig. 23, an equivalent of the semiconductor device SGC3 is described. The fourth and fifth FETS Tr24 and Tr25 are functions as an impedance matching.

Referring to Figs. 17 and 18, the gain control voltage dependency of the gain and the gain compression dependency of the IMD3 in the semiconductor device SGC3 described below. The characteristics represented in these figures are obtained from the experiments executed under the condition that the power supply voltage is 5 V, the gain control voltage applied to the gain control terminal 300 is varied from 2.0 to 3.0 V, the gate width wg of each of the first, second, and third FETs Tr21, Tr22, Tr23 is 250 μm, the gate width wg of the fourth and fifth FETs Tr24, Tr25 is 500 μm, the bias-setting damping resistor R21 and gain clamp resistor R22 are both 1 kΩ, and the current clamp resistance R23 is 10 kΩ. A 1000 pF coupling capacitor is connected between the coupling capacitor terminal 800 and the input terminal 100.

As shown in Fig. 17, with the semiconductor device SGC3 of Fig. 6, it is possible to control the gain from +14 dB to -22 dB with respect to the gain control voltage from 2.0 V to 3.0 V. In other words, the variation from the voltage for obtaining the maximum gain to the voltage for obtaining the minimum gain is between the power supply voltage and the ground voltage of the gain control circuit. Thus, it is not necessary to provide a separate power supply for controlling the gain control. It is to be noted that the measured frequency is 400 MHz, and the maximum saturation drain current I_{DSS} obtained in the above case is 8.9 mA.

The gain compression dependency of the third order intermodulation distortion suppression ratio is shown in Fig. 18. The third order intermodulation distortion component is the 350 MHz third order intermodulation distortion output component produced when two signals (400 MHz and 450 MHz) are input at a -30 dBm input level. The signal component is the output component when a 400 MHz signal is input at a -30 dBm input level. As will be known from Fig. 18, third order intermodulation distortion product performance of greater than 60 dBc is obtained within a range from zero to 10 dB of gain compression.

As described hereinabove, a gain control circuit and a semiconductor device according to the present invention can set a sufficient drain to source voltage to operate each of the FETs in the saturation range, feature low third order intermodulation distortion product characteristics, and can simultaneously obtain both sufficient gain and a stable DC bias even when there is significant variation in the maximum saturation drain current and the power supply voltage is low. It is also not necessary to provide a separate power supply for gain control because the voltage range required to obtain the maximum and minimum gain levels is between the ground voltage and the power supply voltage of the gain control circuit.

In addition, the semiconductor device integrating this gain control circuit has few external terminals and requires few external components, and can therefore contribute to improved efficiency in the assembly process.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and modifications are to be understood as included within the scope of the present invention as defined by the appended claims unless they depart therefrom.

Claims

1. A gain control circuit (GC1) comprising:

a first FET (Tr1) for serving as an active load connected to a power supply line (ps);

a second FET (Tr2) for serving as an amplifier arranged in a series connection with said first FET (Tr1);

a third FET (Tr3) for serving as a current source arranged in a series connection with said second FET (Tr2);

a fourth FET (Tr4) for serving as a variable active load arranged in a parallel connection with said third FET (Tr3), said fourth FET (Tr4) being connected to a gain control line (300); and

a capacitor (C1) connected between said third and fourth FETs (Tr3 and Tr4), whereby the gain of said second FET (Tr2) is controlled by the voltage applied to the gate (g4) of said fourth gate (g4) through said gain control line (300).

2. A gain control circuit (GC1) comprising:

a first FET (Tr1) having a first gate (g1), a first drain (d1) connected to a power line (ps), and a first source (s1) connected to said first gate (g1), said first FET (Tr1) serving as an active load;

a second FET (Tr2) having a second gate (g2), a second drain (d2) connected to said first source (s1), and a second source (s2), said second FET (Tr2) serving as an amplifier;

a resistor (R1) connected between said second gate (g2) and said second source (s2), said resistor (R1) serving as a damping resistor for setting the bias;

a third FET (Tr3) having a third gate (g3), a third drain (d3) connected to said second source (s2), a third source (s3) connected to said third gate (g3), said third source (s3) and said third gate (g3) being grounded, said third FET (Tr3) serving as a current source, said first, second, and third FETs (Tr1, Tr2, and Tr3) having substantially the same characteristics;

a fourth FET (Tr4) having a fourth gate (g4) connected to a gain control line (300), a fourth drain (d4) connected to said second source (s2), and a fourth source (s4), said fourth FET (Tr4) serving as a variable active load; and

a capacitor (C1) connected between said third source (s3) and said fourth source (s4), whereby the gain of said second FET (Tr2) serving as an amplifier is controlled by the voltage applied to said fourth gate (g4) through said gain control line (300).

3. A gain control circuit (GC2) comprising:

a first FET (Tr11) having a first gate (g11), a first drain (d11) connected to a power line (ps), and a first source (s11) connected to said first gate (g11), said first FET (Tr11) serving as an active load;

a second FET (Tr13) having a second gate (g13) connected to a gain control line (300), a second drain (d13) connected to said first source (s11), and a second source (s13), said second FET (Tr13) serving as a variable active load;

a third FET (Tr12) having a third gate (g12), a third drain (d12) connected to said second source (s13), and a second source (s12) connected to a ground, said third FET (Tr12) serving as an amplifier, said first, second, and third FETs (Tr11, Tr13, and Tr12) having substantially the same characteristics;

a capacitor (C11) connected between said first drain (d11) and said first source (s11), said capacitor serving as a high frequency ground capacitor;

a choke coil (L11) connected between said second drain (d13) and said second source (s13); and

a resistor (R11) connected between said third gate (g12) and said third source (s12), said resistor (R11) serving as a damping resistor for setting the bias, whereby the gain of said third FET (Tr12) serving as an amplifier is controlled by the voltage applied to said second gate (g13) through said gain control line (300).

4. A gain control circuit (GC3) comprising:

a first FET (Tr21) having a first gate (g21), a first drain (d21) connected to a power line (ps), and a first source (s21) connected to said first gate (g21), said first FET (Tr21) serving as

an active load;

a second FET (Tr23) having a second gate (g23) connected to a gain control line (300), a second drain (d23) connected to said first source (s21), and a second source (s23), said second FET (Tr23) serving as a variable active load;

a third FET (Tr22) having a third gate (g22), a third drain (d22) connected to said first source (s21), and a third source (s22) connected to a ground, said third FET (Tr22) serving as an amplifier, said first and third FETs (Tr21 and Tr22) having substantially the same characteristics;

a capacitor (C21) connected between said second source (s23) and said third gate (g22);

a resistor (R21) connected between said third gate (g22) and said third source (s22), said resistor (R21) serving as a damping resistor for setting the bias, whereby the gain of said third FET (Tr22) serving as an amplifier is controlled by the voltage applied to said second gate (g23) through said gain control line (300).

5. A semiconductor device (SGC1) comprising:

a first FET (Tr1) having a first gate (g1), a first drain (d1) connected to a power line (600), and a first source (s1) connected to said first gate (g1), said first FET (Tr1) serving as an active load;

a second FET (Tr2) having a second gate (g2), a second drain (d1) connected to said first source (s1), and a second source (s2), said second FET (Tr2) serving as an amplifier;

a first resistor (R1) connected between said second gate (g2) and said second source (s2), said first resistor (R1) serving as a damping resistor for setting the bias;

a third FET (Tr3) having a third gate (g3), a third drain (d3) connected to said second source (s2), a third source (s3) connected to said third gate (g3), said third source (s3) and said third gate (g3) being grounded, said third FET (Tr3) serving as an rated current source, said first, second, and third FETs (Tr1, Tr2, and Tr3) having substantially the same characteristics;

a fourth FET (Tr4) having a fourth gate (g4) connected to a gain control line (300), a fourth drain (d4) connected to said second source (s2), and a fourth source (s4) grounded through a capacitor (C1), said fourth FET (Tr4) serving as a variable active load;

a second resistor (R2) connected between said fourth drain (d4) and said fourth source (s4), said second resistor (R2) serving as a gain clamper;

a third resistor (R3) connected between said fourth gate (g4) and said gain control line (300), said third resistor (R3) serving as a current clamper;

a fifth FET (Tr5) having a fifth gate (g5) connected to said first source (s1), a fifth drain (d5) connected to said first drain (d1), and a fifth source (s5), said fifth FET (Tr5) serving as a source follower; and

a sixth FET (Tr6) having a sixth gate (g6), a sixth drain (d6) connected to said fifth source (s5), and a sixth source (s6) connected to said sixth gate (g6), said sixth FET (Tr6) serving as a rated current source, whereby the gain of said second FET (Tr2) serving as an amplifier is controlled by the voltage applied to said fourth gate (g4) through said gain control line (300).

6. A semiconductor device (SGC2) comprising:

a first FET (Tr11) having a first gate (g11), a first drain (d11) connected to a power line (600), and a first source (s11) connected to said first gate (g11), said first FET (Tr11) serving as an active load;

a second FET (Tr13) having a second gate (g13), a second drain (d13) connected to said first source (s11), and a second source (s13), said second FET (Tr13) serving as a variable active load;

a first resistor (R11) between said second gate (g13) and a gain control line (300), said gain control line connected to said first source (s11) through a capacitor (C11) and to said second source (s13) through a choke coil (L11);

a third FET (Tr12) having a third gate (g12), a third drain (d12) connected to said second source (s13), and a third source (s12) connected to a ground (500), said third FET (Tr12) serving as an amplifier, said first, second, and third FETs (Tr11, Tr13, and Tr12) having substantially the same characteristics;

a second resistor (R11) connected between said third gate (g12) and said third source (s12), said second resistor (R11) serving as a damping resistor for setting the bias;

a fourth FET (Tr14) having a fourth gate (g14) connected to said second source (s13), a fourth drain (d14) connected to said first drain (d11), and a fourth source (s14); and

a fifth FET (Tr15) having a fifth gate (g15) connected to said third source (s12), a fifth drain (d15) connected to said fourth source (s14), and a fifth source (s15) connected to said fifth gate (g15), whereby the gain of said third FET (Tr12) serving as an amplifier is controlled by the voltage applied to said sec-

ond gate (g13) through said gain control line (300).

7. A semiconductor device (SGC3) comprising:

a first FET (Tr21) having a first gate (g21), a first drain (d21) connected to a power line (600), and a first source (s21) connected to said first gate (g21), said first FET (Tr21) serving as an active load;

a second YET (Tr23) having a second gate (g23), a second drain (d23) connected to said first source (s21), and a second source (s23), said second FET (Tr23) serving as a variable active load;

a third FET (Tr22) having a third gate (g22) connected to said second source (s23) through an capacitor (C21), a third drain (d22) connected to said first source (s21), and a second source (s22) connected to a ground (500), said third FET (Tr22) serving as an amplifier, said first and third FETs (Tr21 and Tr22) having substantially the same characteristics;

a fourth FET (Tr24) having a fourth gate (g24) connected to said third drain (d22), a fourth drain (d24) connected to said first drain (d21), and a fourth source (s24), said fourth FET (Tr24) serving as a source follower,

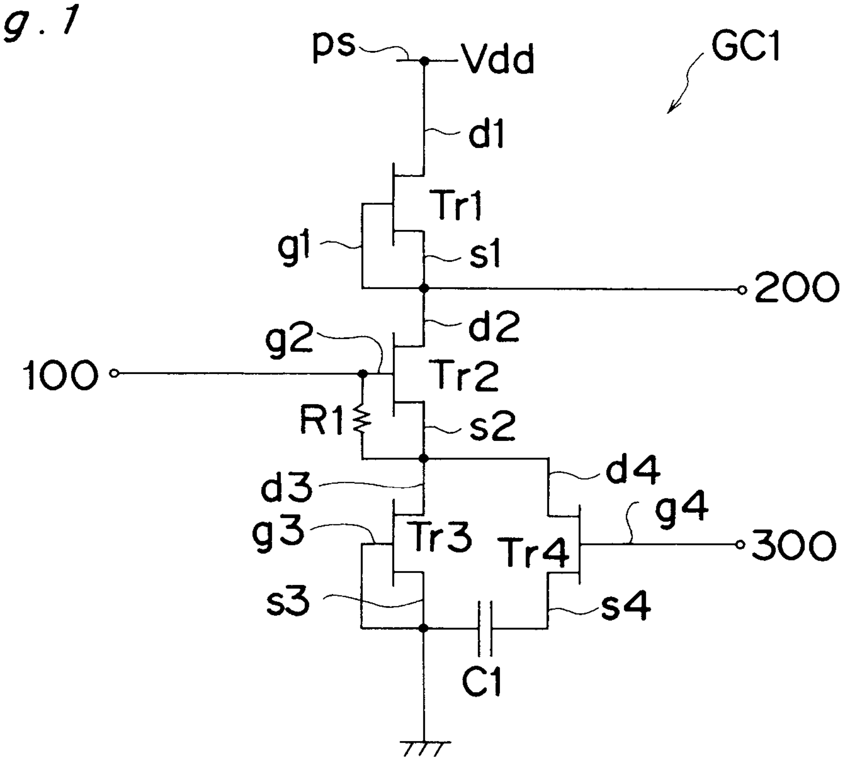
a fifth FET (Tr25) having a fifth gate (g25) connected to said third source (s22), a fifth drain (d25) connected to said fourth source (s24), and a fifth source (s25) connected to said fifth gate (g25), said fifth FET (Tr25) serving as a rated current source;

a first resistor (R21) connected between said third gate (g22) and said third source (s22), said resistor (R1) serving as a damping resistor for setting the bias;

a second resistor (R22) connected between said second source (s23) and said fourth drain (d22), said second resistor (R22) serving as a gain clamper; and

a third resistor (R23) connected between said second gate (g23) and a gain control line (300), said third resistor (R23) serving as a current clamper, whereby the gain of said third FET (Tr22) serving as an amplifier is controlled by the voltage applied to said second gate (g23) through said gain control line (300).

Fig.1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Vdd
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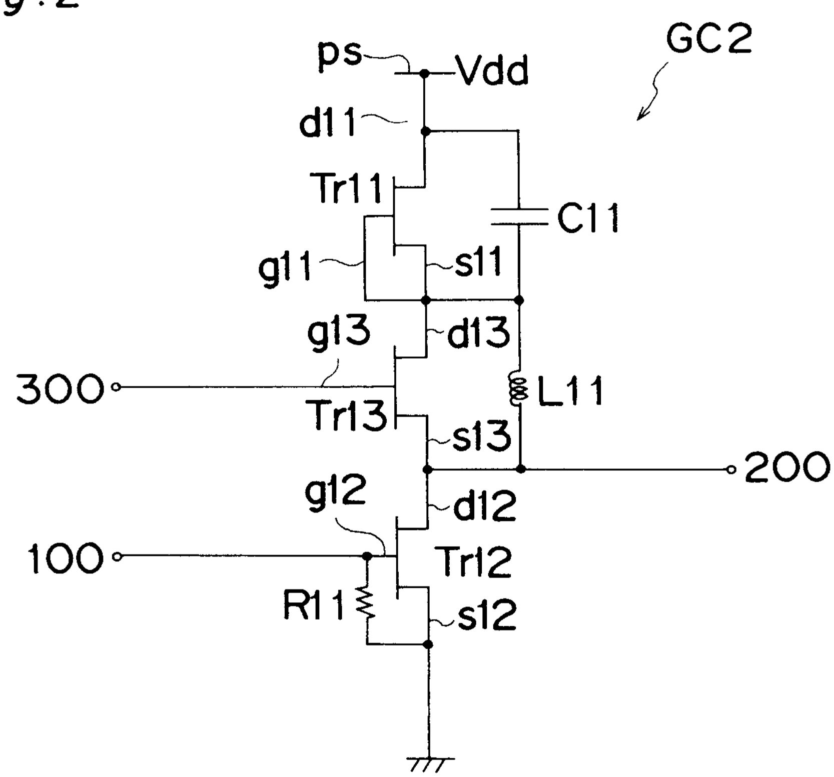
d1
Tr1
g1
s1
200
g2
d2
100
Tr2
R1
s2
d3
d4
g4
g3
Tr3
Tr4
300
s3
s4
C1

Fig.2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Vdd
GC2
d11
Tr11
C11
g11
s11
g13
d13
300
L11
Tr13
s13
200
g12
d12
100
Tr12
R11
s12

Fig.3

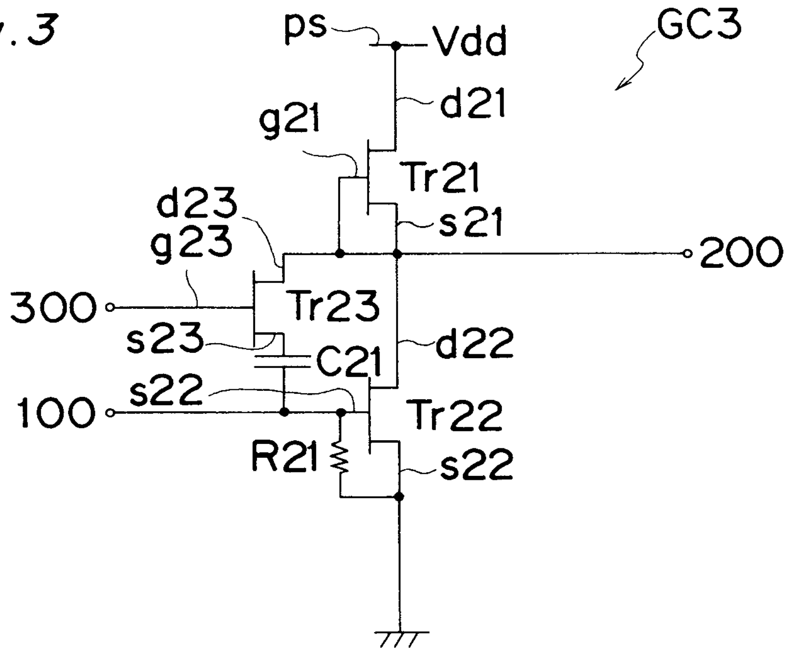

ps
Vdd
GC3
d21
g21
Tr21
d23
g23
s21
200
300
Tr23
s23
C21
d22
s22
100
Tr22
R21
s22

Fig.4

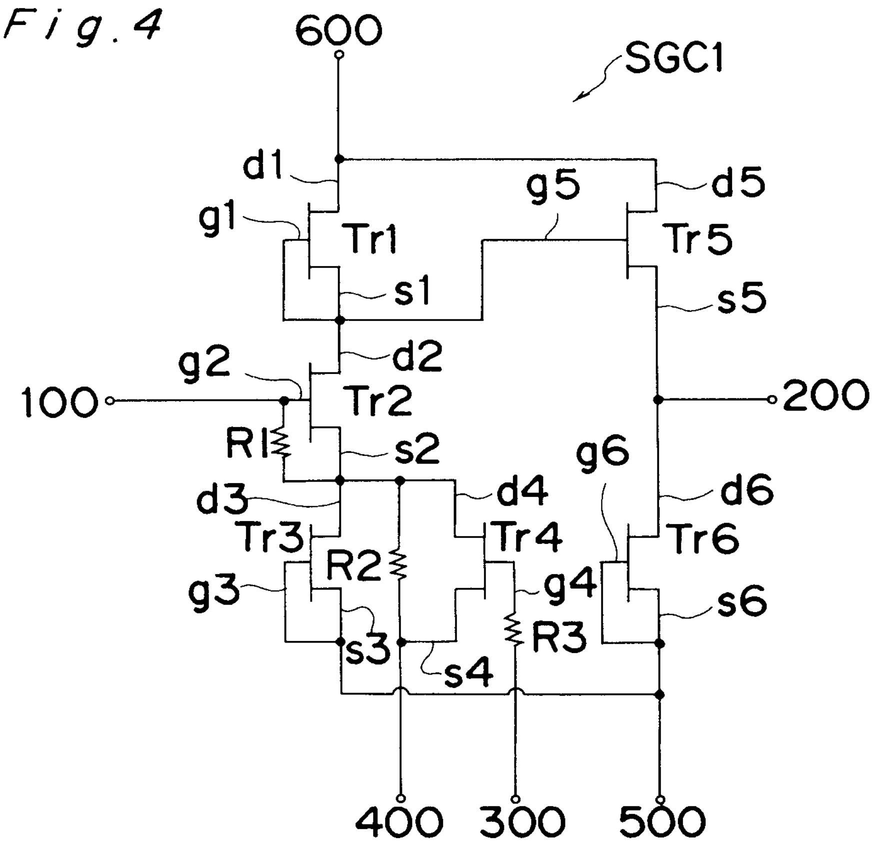

600
SGC1
d1
d5
g5
g1
Tr1
Tr5
s1
s5
d2
g2
100
Tr2
200
R1
s2
g6
d3
d4
d6
Tr3
Tr4
Tr6
R2
g3
g4
s6
R3
s3
s4
400
300
500

Fig. 5

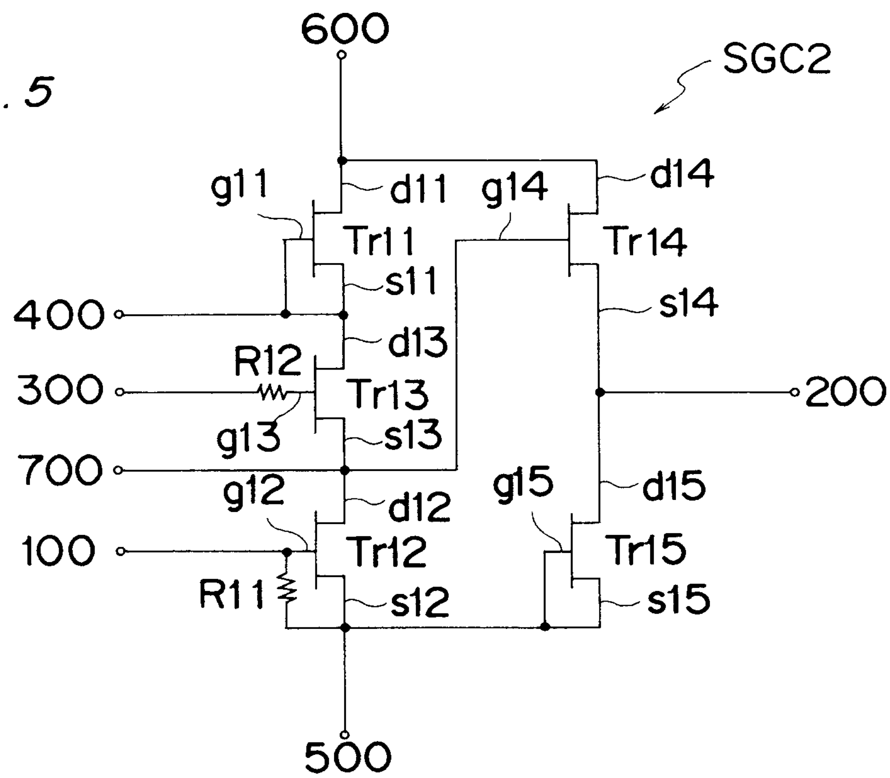

600
SGC2
g11
d11
g14
d14
Tr11
Tr14
s11
s14
400
d13
R12
300
Tr13
200
g13
s13
700
g15
g12
d15
d12
Tr12
Tr15
100
R11
s12
s15
500

Fig. 6

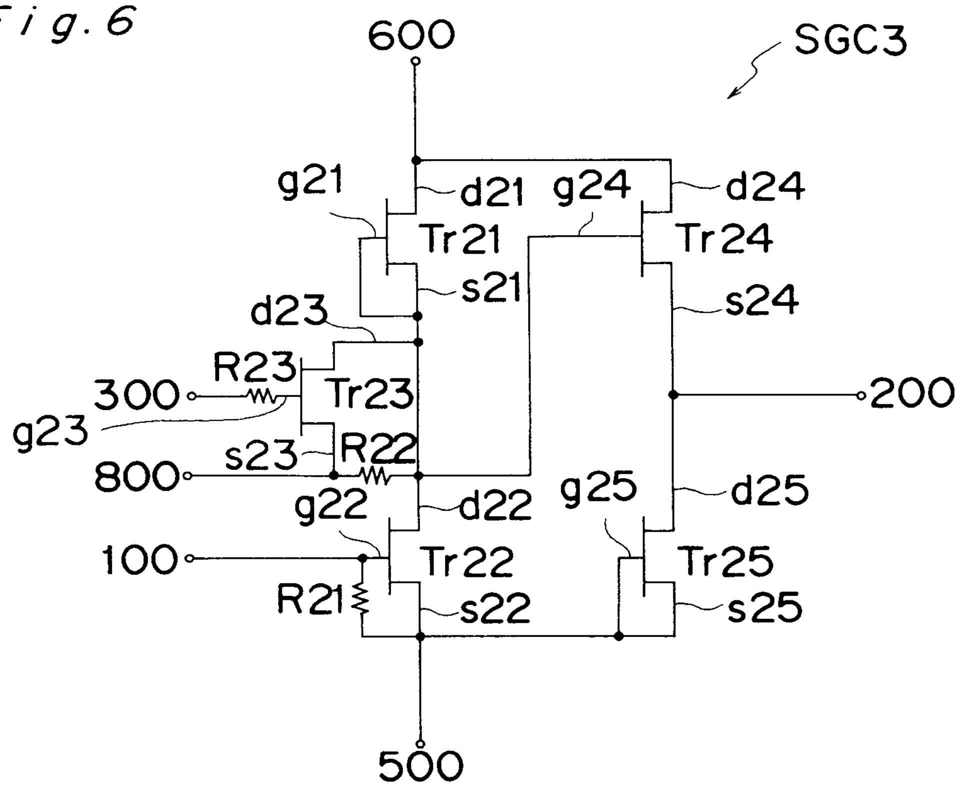

600
SGC3
g21
d21
g24
d24
Tr21
Tr24
s21
s24
d23
R23
300
Tr23
200
g23
s23
R22
800
g25
g22
d22
d25
100
Tr22
Tr25
R21
s22
s25
500

Fig.7

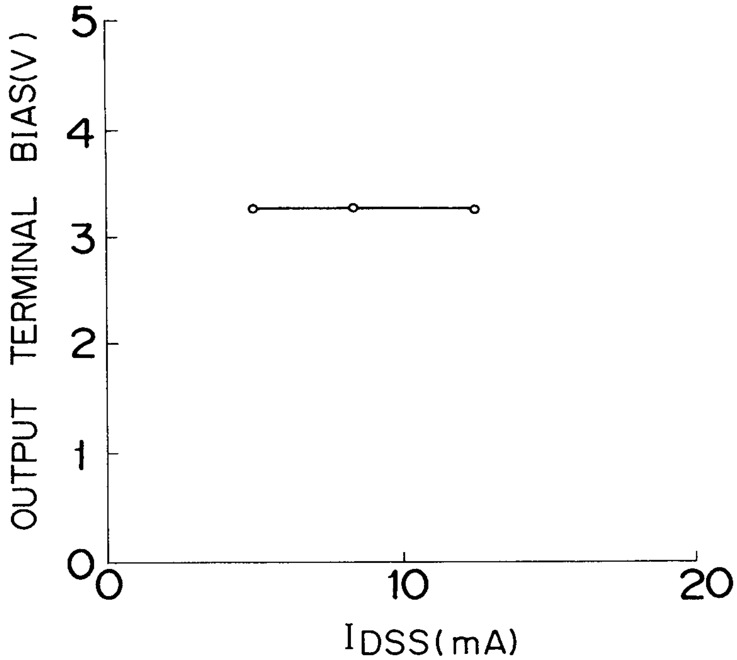

OUTPUT TERMINAL BIAS(V)
0
1
2
3
4
5
0
10
20
IDSS(mA)

Fig.8

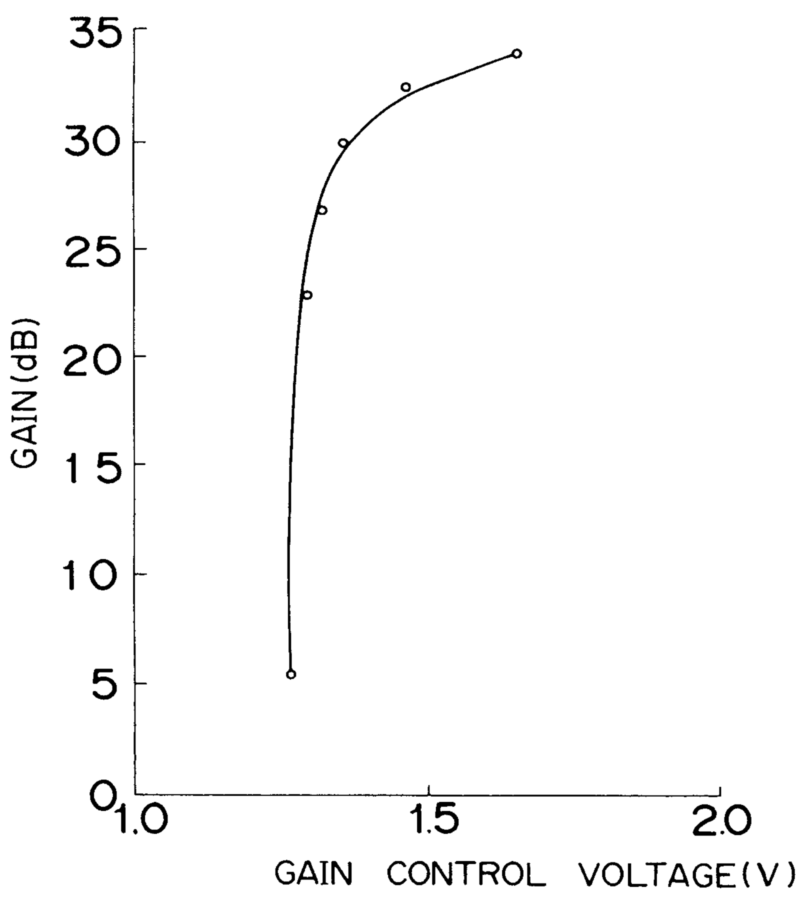

GAIN(dB)
0
5
10
15
20
25
30
35
1.0
1.5
2.0
GAIN CONTROL VOLTAGE(V)

Fig.9

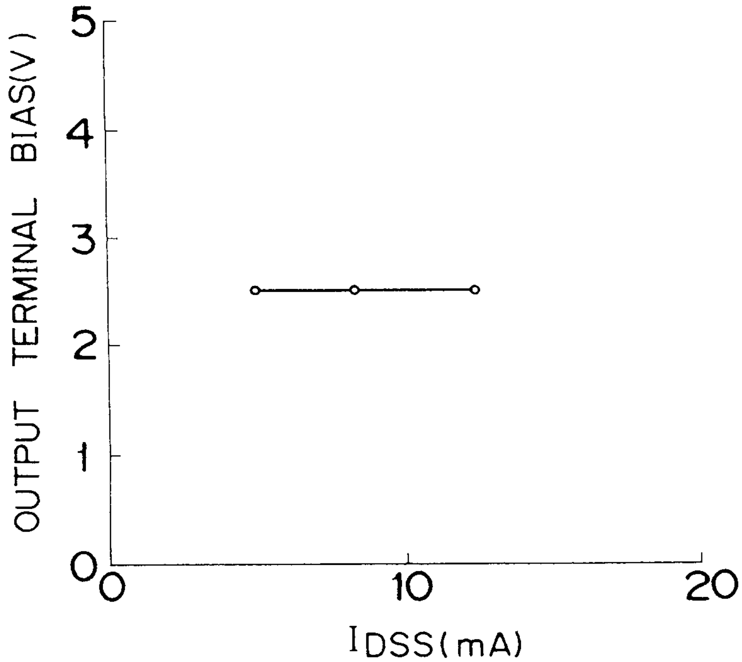

5
4
3
2
1
0
OUTPUT TERMINAL BIAS(V)
0
10
20
IDSS(mA)

Fig.10

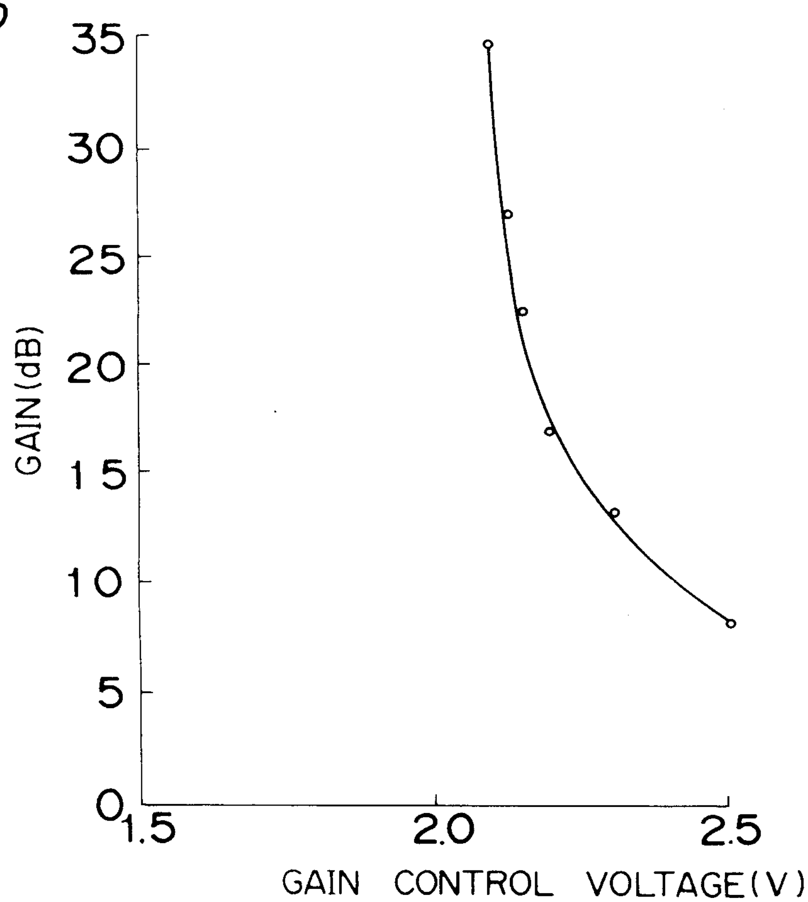

35
30
25
20
15
10
5
0
GAIN(dB)
1.5
2.0
2.5
GAIN CONTROL VOLTAGE(V)

Fig.11

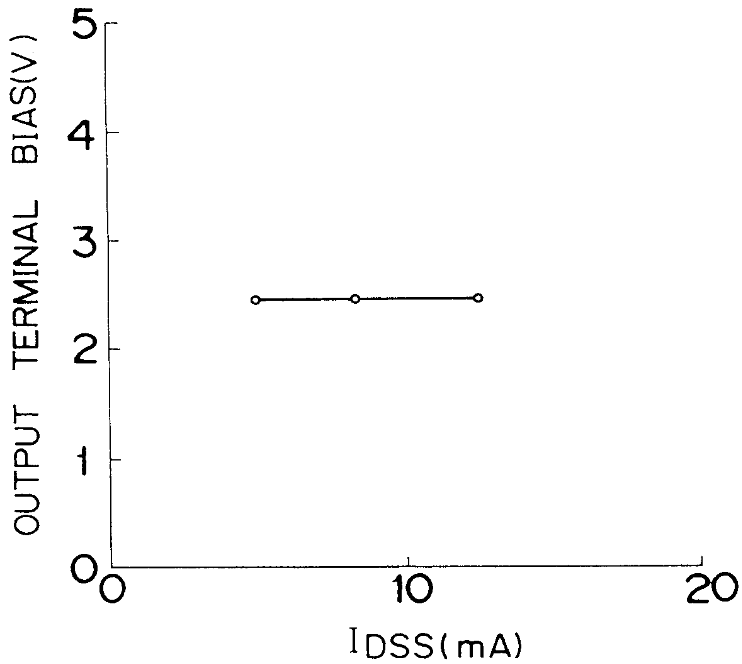

OUTPUT TERMINAL BIAS(V)
5
4
3
2
1
0
0
10
20
IDSS(mA)

Fig.12

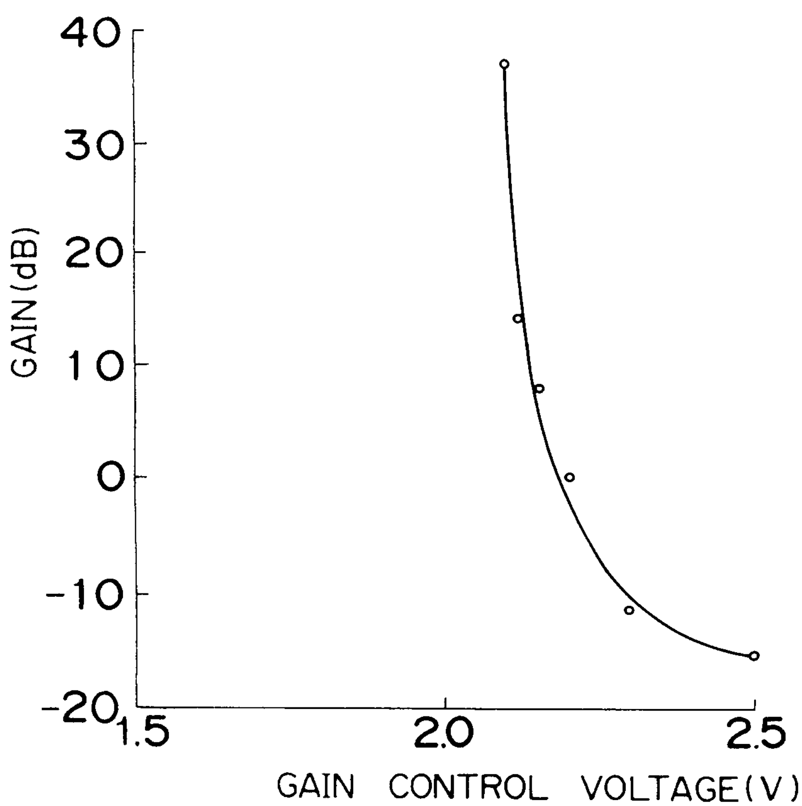

GAIN(dB)
40
30
20
10
0
-10
-20
1.5
2.0
2.5
GAIN CONTROL VOLTAGE(V)

Fig.13

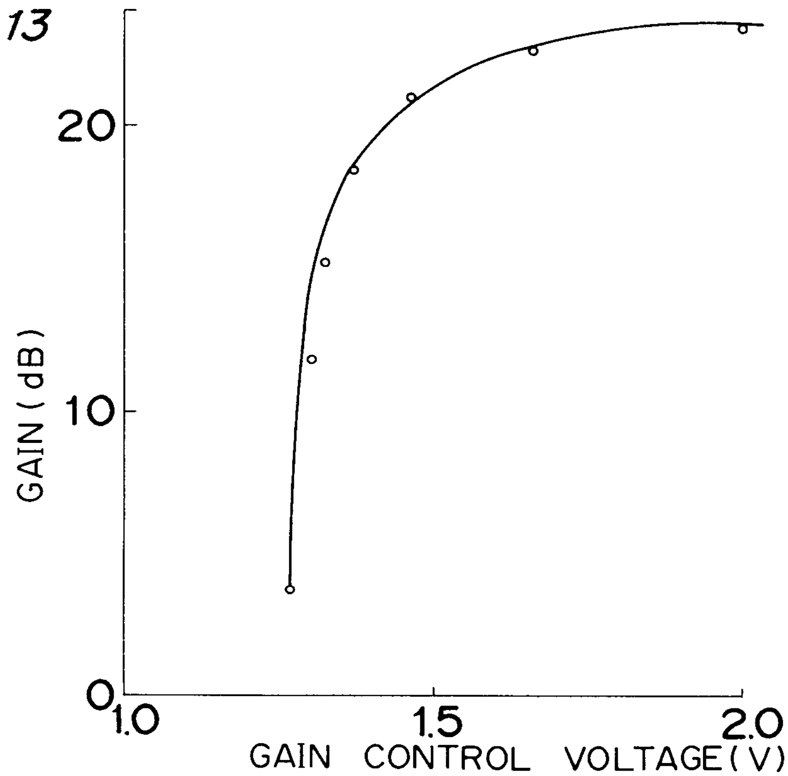

GAIN (dB)
20
10
0
1.0
1.5
2.0
GAIN CONTROL VOLTAGE (V)

Fig.14

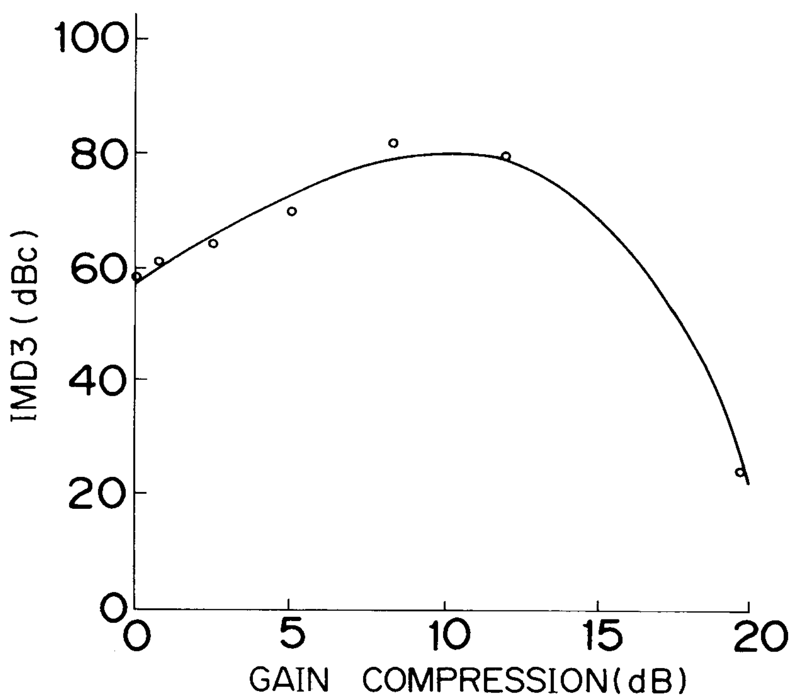

IMD3 (dBc)
100
80
60
40
20
0
0
5
10
15
20
GAIN COMPRESSION (dB)

Fig.15

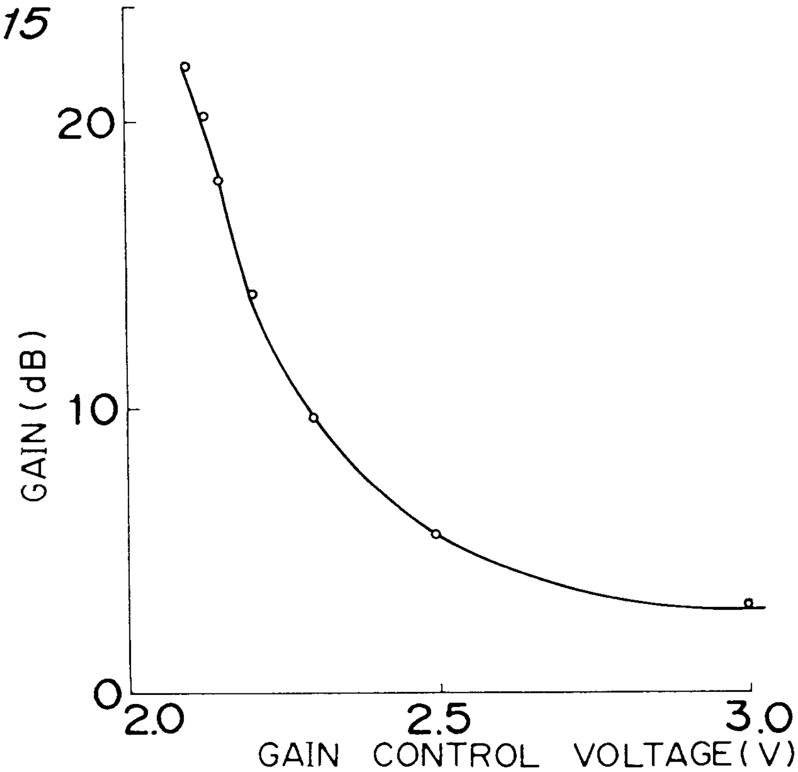

GAIN (dB)
20
10
0
2.0
2.5
3.0
GAIN CONTROL VOLTAGE (V)

Fig.16

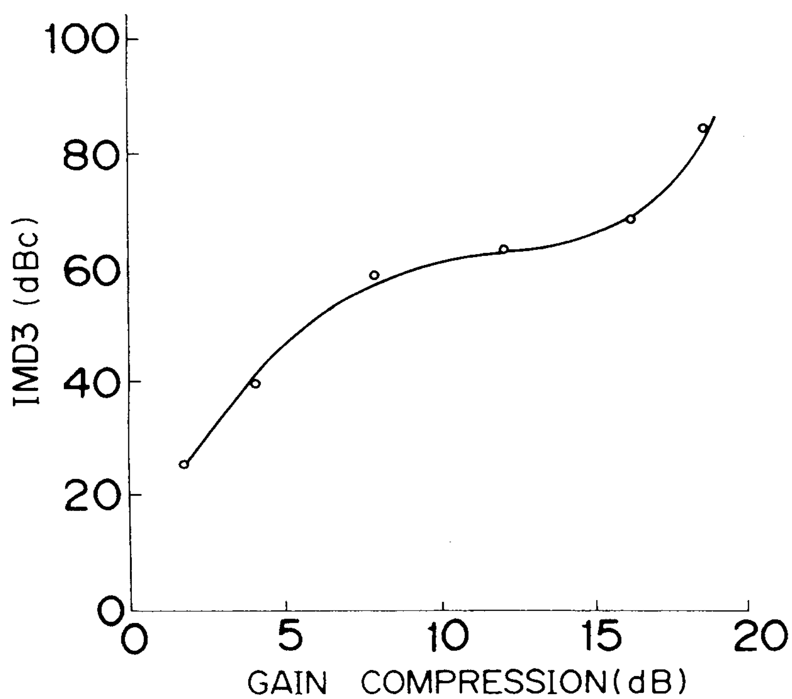

IMD3 (dBc)
100
80
60
40
20
0
0
5
10
15
20
GAIN COMPRESSION (dB)

Fig.17

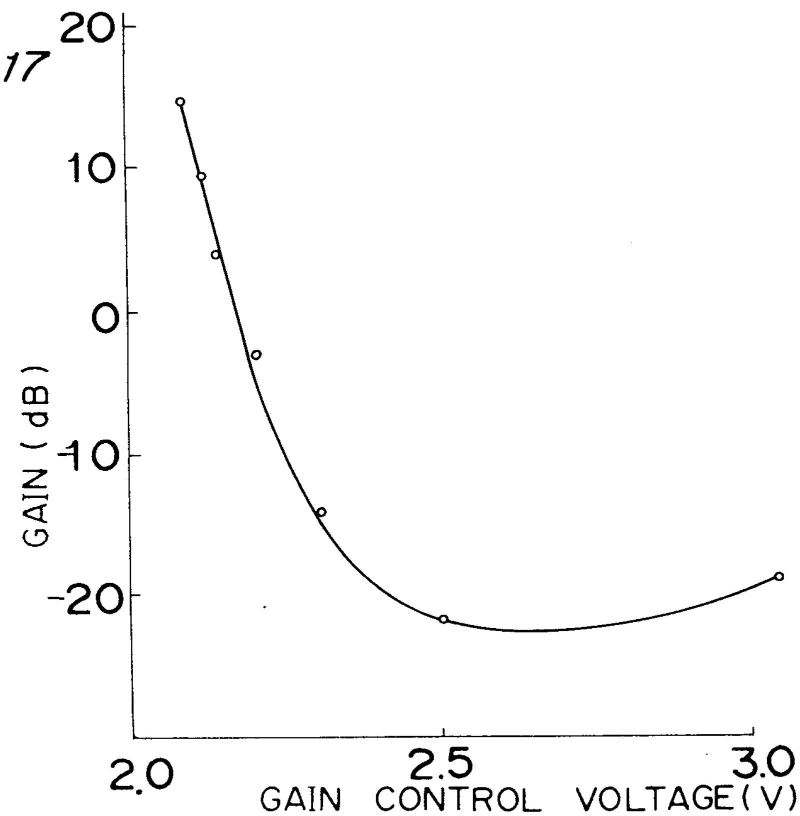

20
10
0
-10
-20
GAIN (dB)
2.0
2.5
3.0
GAIN CONTROL VOLTAGE(V)

Fig.18

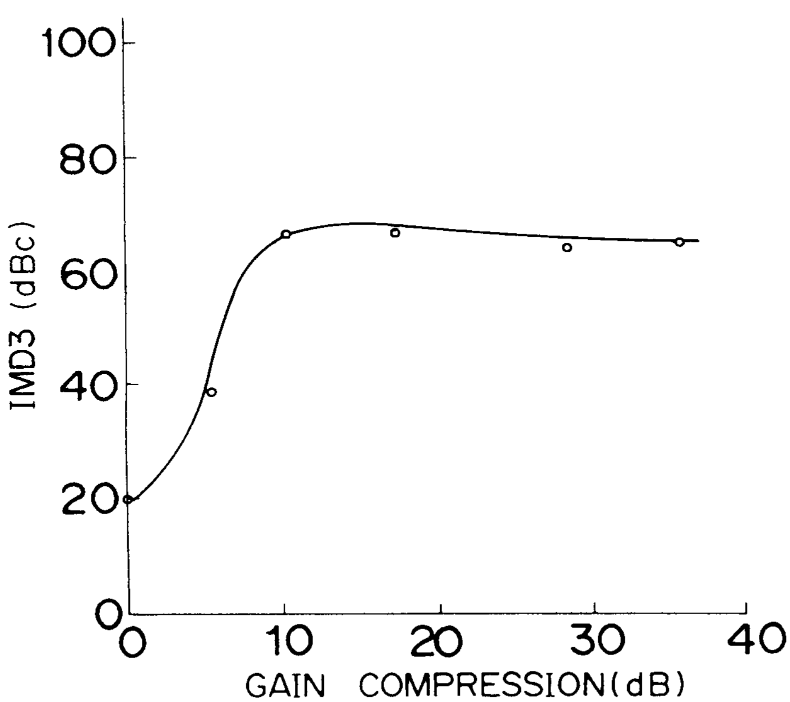

100
80
60
40
20
0
IMD3 (dBc)
0
10
20
30
40
GAIN COMPRESSION(dB)

Fig.19

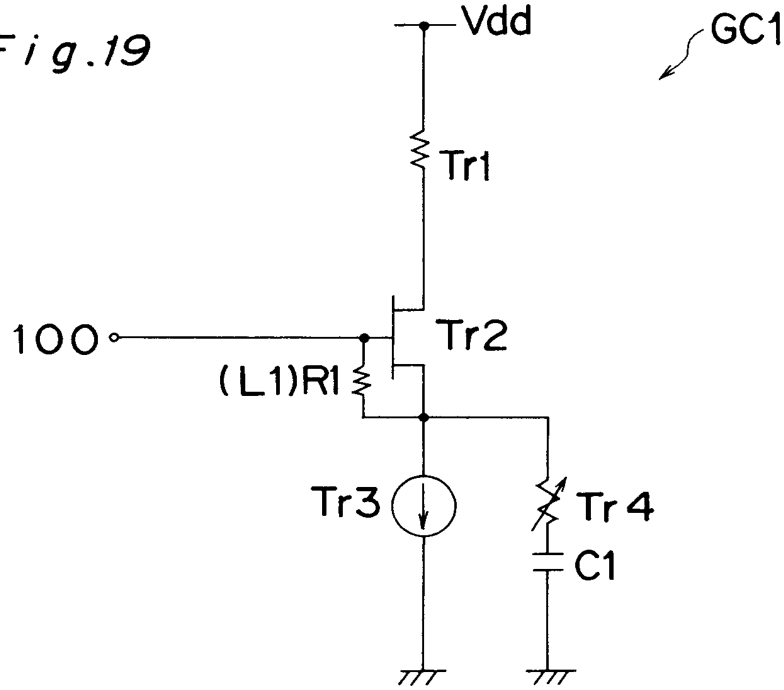

Vdd
GC1
Tr1
100
Tr2
(L1)R1
Tr3
Tr 4
C1

Fig. 20

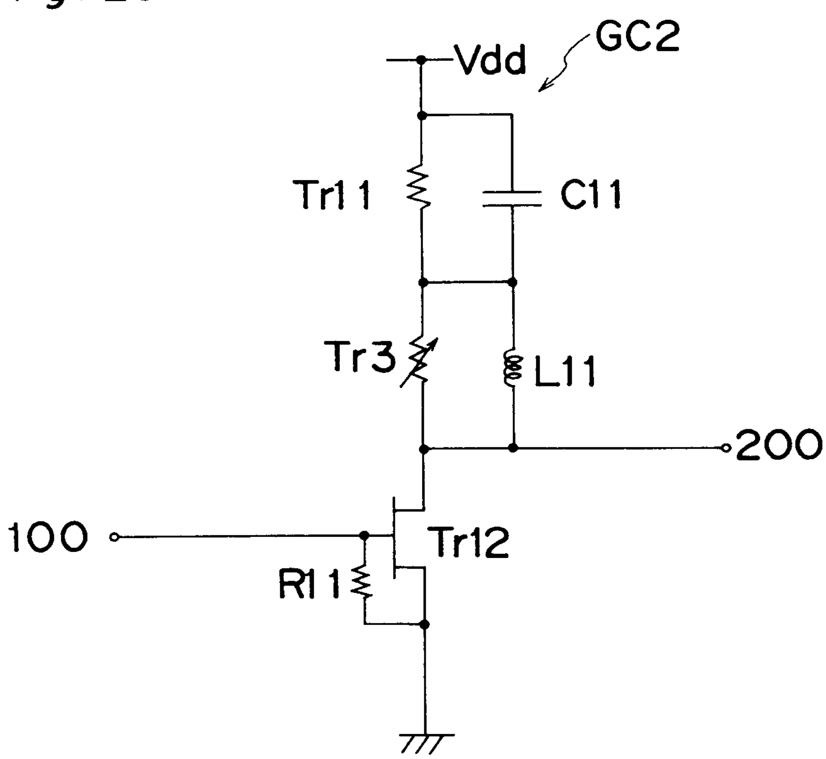

Vdd
GC2
Tr1 1
C11
Tr3
L11
200
100
Tr12
R1 1

Fig. 21

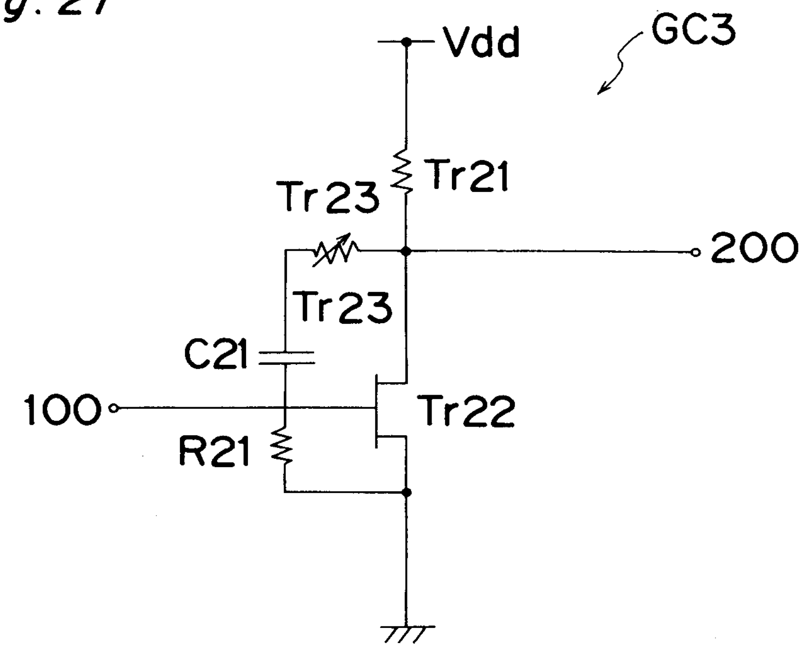

Vdd
GC3
Tr21
Tr23
200
Tr23
C21
100
Tr22
R21

Fig. 22

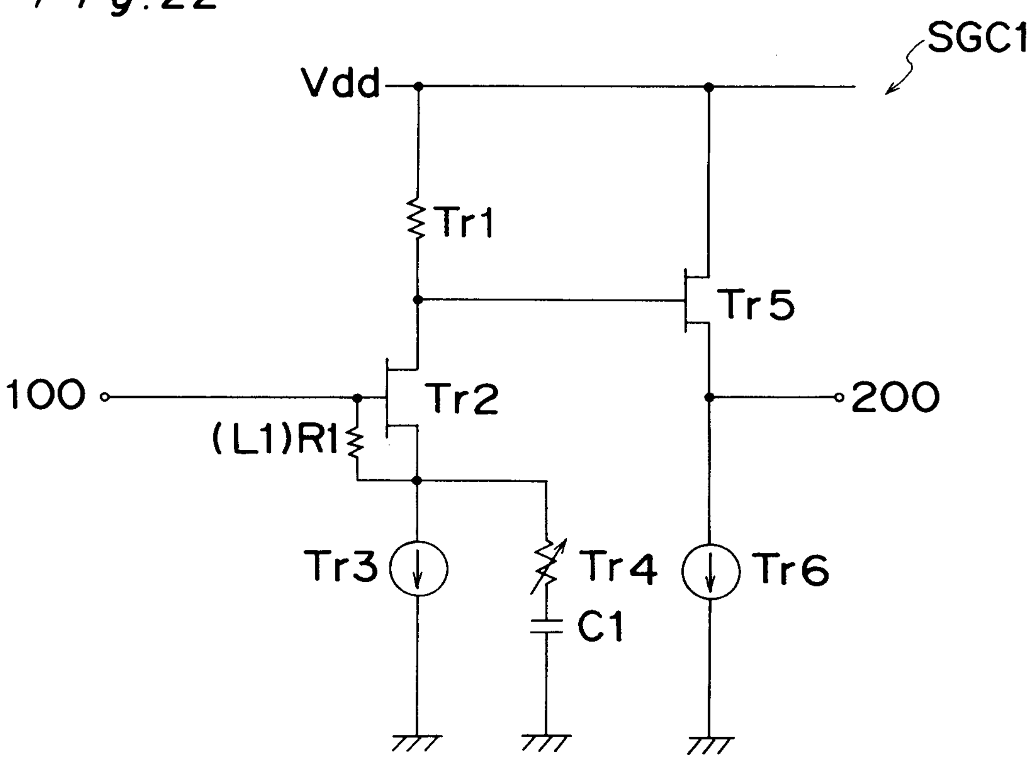

SGC1
Vdd
Tr1
Tr5
100
Tr2
200
(L1)R1
Tr3
Tr4
Tr6
C1

Fig. 23

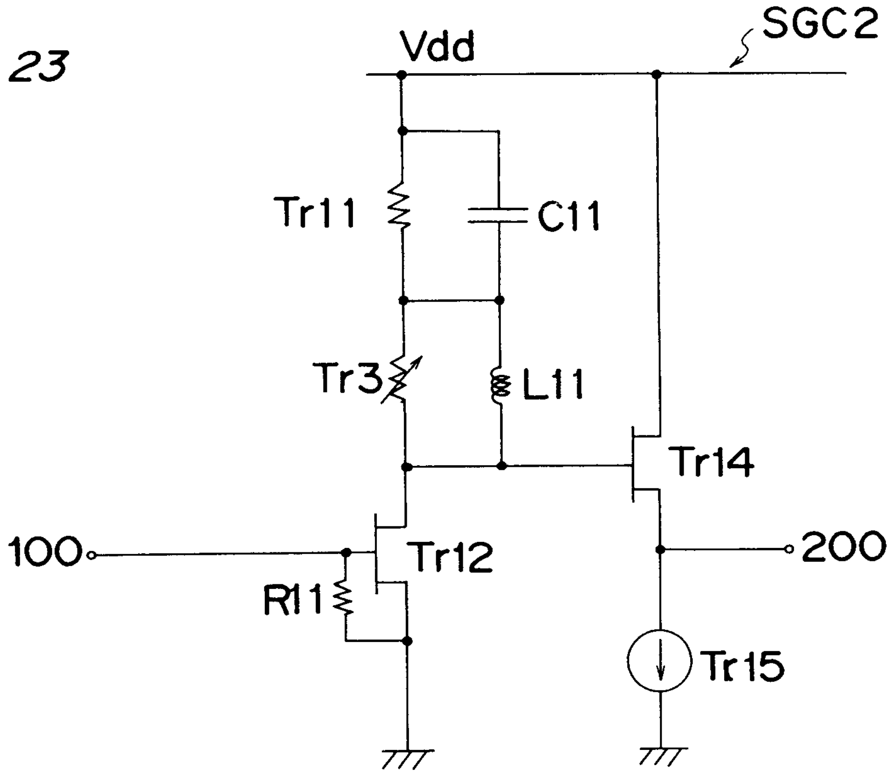
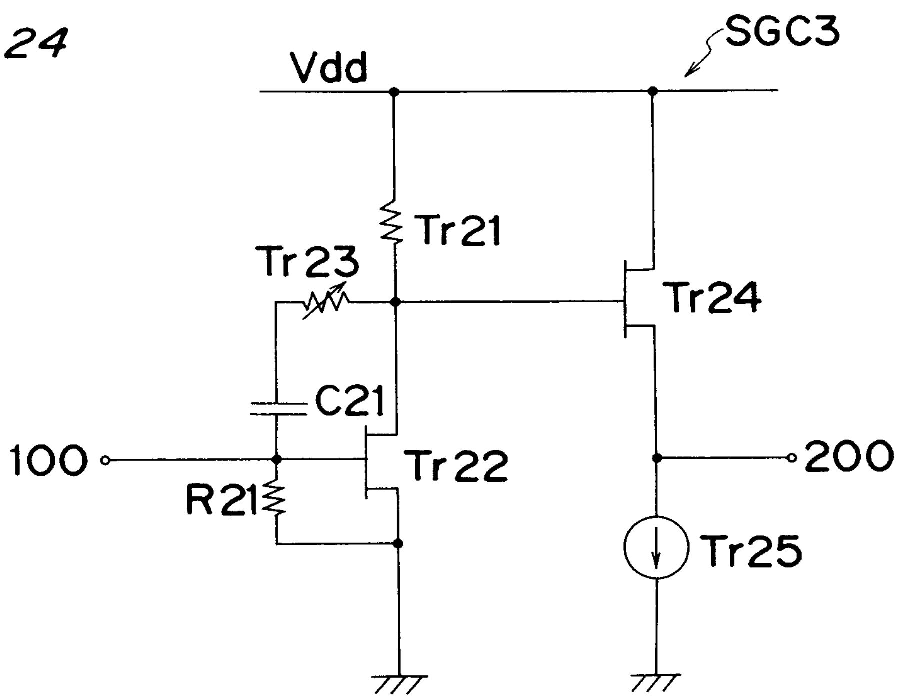

Vdd
SGC2
Tr11
C11
Tr3
L11
Tr14
100
Tr12
200
R11
Tr15

Fig. 24


Vdd
SGC3
Tr21
Tr23
Tr24
C21
100
Tr22
200
R21
Tr25